

8088 CPU Tester

The 8088 CPU Tester is used to test an 8088 CPU running at 16 MHz. It checks address and data bus functionality, NMI (Non-Maskable Interrupt) operation, CPU instruction execution, and counter functions. Although these tests do not cover every function of the 8088, they provide confidence that the CPU and supporting logic are operating correctly.

1. Usage

1. Remove power from the CPU Tester.
2. Install the 8088 CPU into the ZIF socket, observing the correct orientation.
3. Apply 5V power to the board and observe the LEDs.
4. Read the result:
 - the LEDs light one after another until all eight are lit, then one LED runs up and down continuously — **PASS**: the CPU passed every test;
 - the LEDs stop lighting and one LED flashes — **FAIL**. Note which LED is flashing: it marks the test the CPU failed.
 - no LED lights at all — the CPU never fetched an instruction.

Testing a CPU quickly

Interpreting a failure is not necessary in order to test a CPU. A pass is unambiguous: the running LED indicates a working CPU.

2. No LEDs lit

If all eight LEDs remain off, the CPU never fetched an instruction, so is likely faulty.

3. What each LED means

Each LED stands for one test, in the order the firmware runs them. Once a test has passed, its LED stays lit and the next test starts:

LED	Test
D0	The CPU started up and reached the test function
D1	Check EPROM - this verifies address/data buses and decoding logic
D2	Test SRAM - this verifies address/data buses and decoding logic and stack.
D3	Same as above
D4	Test 8255 I/O - Reading and writing ports
D5	Test 8253 PIT and CPU counters
D6	Additional testing of CPU counters
D7	Test CPU NMI

4. What the tests do

The firmware runs eight tests in the order below. Each test exercises more of the CPU than the preceding one and lights one further LED.

Test 1 — start-up (D0)

The first action of the firmware is to install an NMI vector so that an interrupt cannot divert execution, to configure the 8255 for *PA out, PB out, all of port C an input* (control word 89h), to drive PB low once, and to park 8253 counter 1 in mode 1 so that its output remains inactive. It then lights D0. Reaching this point proves that the CPU reset cleanly, fetched from the reset vector and executed a sequence of instructions.

Test 2 — EPROM checksum (D1)

Every 16-bit word of the 64 K image is summed and the total must be zero. The final two bytes of the image are set at build time to make this so. The test therefore exercises the CPU's address and data buses and the whole EPROM, rather than a single location.

Test 3 — SRAM, data patterns (D2)

The SRAM window 0000h-3FFFh is written with all zeros and read back, then with all ones and read back. This detects stuck and shorted data bits.

Test 4 — SRAM, addressing (D3)

Three patterns are written to every location and verified: the low address byte, its complement, and a pattern derived from address bits A12-A8. Address bit A13 is the chip's alias select and is masked out. This detects stuck, open or shorted address lines, a fault that the data test can miss entirely.

Test 5 — 8255 port C, the strap test (D4)

Port C of the 8255 is connected to fixed pull-up and pull-down straps, so with port C configured as an input it must read a fixed, known value.

Test 6 — 8253 counter 0 (D5)

Counter 0 is loaded with FFFFh in mode 0 and read back twice with a delay between the reads: the count must have decreased, and by an amount within the expected range. This exercises the clock input, the gate, the control register and the counter itself — in effect, the complete CPU-to-8253 write and read path.

Test 7 — 8253 counter 2 (D6)

The same test is applied to counter 2, so that a single faulty counter cannot be concealed by a working one.

Test 8 — 8253 counter 1 into NMI (D7)

Counter 1 is programmed as a rate generator (mode 3) driven from the processor clock, and its OUT1 output is wired to the 8088's NMI input. The firmware counts the interrupts serviced by its NMI handler over approximately one quarter of a second and requires at least twenty. This is the only test that exercises the CPU's non-maskable interrupt input and its interrupt-acknowledge cycle,

which makes it the most comprehensive test on the board. Counter 1 is parked again afterwards, so that the chase loop runs uninterrupted.

Then: the chase (all eight)

Once every test has passed, the firmware runs a single LED up and down continuously. This is the pass indication: the CPU executed the complete test suite and accepted a real interrupt, so the chase indicates a working device.

5. Support

For CPU Testers and technical support: **myretrostore.co.uk**

Manual revisions

Revision	Date	Change
1.0	October 2025	First issue: operation of the tester, all eight tests described, and the 8255 port C strap wiring documented (PC0/2/4/6 to GND, PC1/3/5/7 to +5V; port C reads AAh)